Automatic Generation of Lightweight Controllability and Observability Structures for Analog Circuits

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***Abstract*—In this paper a method is presented to address the automatic testing of analog ICs. Based on Design-for-Testability building blocks offering extra controllability and extra observability, a test infrastructure is generated for a targeted circuit. The selection of the extra blocks and their insertion into the circuit is done automaticaly by a proposed optimization algorithm. Adopting a defect-oriented methodology, this algorithm maximizes the fault coverage and minimizes the silicon area overhead. The proposed method is applied to an industrial circuit to generate an optimal test infrastructure combining controllability and observability. The case study shows that, with a silicon area overhead of less than 10%, a fault coverage of 91% can be reached.**

I. Introduction

The testing of analog Integrated Circuits (ICs) has been a center of focus for many years. And while advances in the domain have been made, the question of testing analog ICs in an automated way still remains. At the same time, electronics has entered or created new markets; and with them new requirements. For instance, the automotive industry combines nowadays an average of 400 ICs per vehicle and intends to increase this number. Since the defect probabilities of all components of a system multiply with each other, the requirement on each component increases and defect level below the part-per-million (ppm) are desired. These quality requirements combined with a shortening time-to-market put pressure on IC designers and manufacturers. Therefore, an advancement is needed in the testing of analog ICs and its automation.

The testing of digital ICs has known an automation of its process and an improvement leading to defect levels under the ppm. This success was made possible by the appearance of automated algorithms such as the D-Algorithm or PODEM [1]. Furthermore, a generic Design-for-Testability (DfT) approach based on flip-flops connected in a scan chain was developed and enabled the automatic utilization of these algorithms.

The problem of testing analog circuits in a generic way has been addressed in works such as [2] [3] where analog scan chains are proposed. In the same way as in digital scan chains, voltages can be scanned through sample-and-hold (S/H) circuits and imposed on node voltages. Similarly, node voltages can be read and scanned out of the chips by chains of S/H circuits. While these methods tackle the testing of analog circuits in a generic approach, they suffer from several drawbacks. The parasitics imposed on the probed nodes by the analog buses have been criticized. Also, the forcing of voltages on internal nodes requires the presence of multiple buffers. The whole approach requires a significant silicon area overhead.

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In this paper a method is proposed to automatically generate a DfT infrastructure in order to test analog ICs. The presented infrastructure combines small building blocks offering extra controllability and extra observability to the circuit under test (CUT). This co-optimization of controllability and observability offers an alternative to the analog scan chains without requiring an excessive silicon area. In Section II, the Defect-Oriented methodology enabling the method is summarized. Then, the building blocks forming the basis of the method are presented in Section III. In Section IV, the algorithm selecting the building blocks through an optimization system is presented. Then, simulation results for an industrial case study are shown in Section V. Finally, conclusions are drawn in Section VI.

II. Defect-Oriented Method

In the defect-oriented approach, the physical defects which can occur in ICs are considered and are simulated with fault models [4]–[6]. Defects can be separated in two categories: catastrophic and parametric defects. The former emerge from a problem during the manufacturing process such as an over- or under-etching, the presence of a dust particle, etc. They cause a modification of the designed topology i.e. a short circuit or an open circuit. The latter emerges from an imperfect control of the process, voltage and temperature (PVT) conditions. These PVT variations cause variability among the produced ICs, resulting in some ICs laying outside of their target specifications. In the scope of this work, the focus is put on automotive applications where the used technologies are typically above 100nm and hence are mastered well enough to apply a 6σ design flow. Therefore, parametric defects are neglected and only catastrophic defects are considered in this work.

The modeling of the defects is done at the schematic level with models used in literature [7] : the 5-fault model for the MOSFETs and the 6-fault model for the bipolar transistors. The application of these models on a circuit C_0 results in a list of faults LF=$\{F_1,...,F_n\}$. Then, one by one, the faults from the generated list LF are inserted into the original circuit C_0. The insertion of a fault F_i in the circuit C_0 leads to the faulty circuit C_i. Therefore, finally n+1 circuits are considered i.e. the original circuit C_0 and the n faulty circuits $\{C_1,...,C_n\}$.

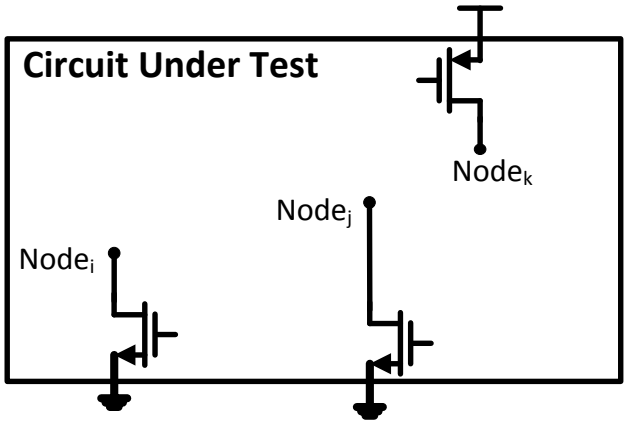

Fig. 1. Block diagram representation of the proposed test infrastructure.

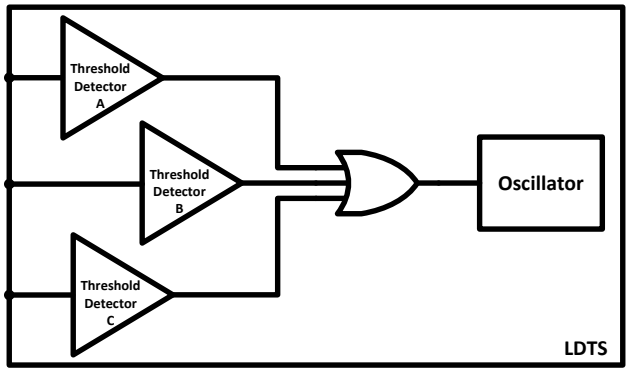

Fig. 2. Internal organization of a LDTS block [7].

These n+1 circuits are simulated with a circuit simulator in the presence of process variations.

III. Controllability and Observability Structures

In this section, the concepts of controllability and observability are introduced as defined in [8]. The controllability is defined as the relative difficulty of setting a node to a specific value. The observability is defined as the relative difficulty of measuring the signal value at a node. The combination of these two concepts forms the basis for an optimized way to test an analog integrated circuit. The main idea is to control a circuit and lead it into a region of operation where a different behavior can be observed between a faulty circuit and a good circuit.

In the following, two techniques are presented to enhance the controllability and the observability of analog ICs. The controllability is enhanced by using the Topology Modification method introduced in [5]. The observability is enhanced by using the Local Detection and Transmission Systems introduced in [7]. Their combination provides a simplification of the test infrastructure proposed by analog scan chains. As a result, DfT Control and Observation Structures (COS) can be generated to test analog ICs with a small silicon area overhead.

A. Topology Modification

The Topology Modification method consists in reconfiguring the targeted CUT to make defects observable. In [9], the modification of the value of some circuits components is used as a form of reconfiguration. In the scope of this work, the topology of the CUT is modified by the means of small transistors added to the original circuit. These transistors are either connected between a node of the circuit and the ground (pull-down transistor), or a node of the circuit and the voltage supply (pull-up transistor) as illustrated in Figure 1. In the following, the distinction between a pull-down (PD) or pull-up (PU) transistor is of no importance. Therefore, the general denomination PX is adopted. The insertion of the PX transistors in the original circuit C_0 leads to a set of topologies $\{\text{TM}_0,...,\text{TM}_p\}$, where TM_0 is the original circuit C_O.

During the normal operation of the circuit, the PXs are deactivated and hence do not have any effect on the circuit, besides the small capacitive parasitics inherent to their presence. During the test mode, these small transistors are independently activated in order to make the CUT adopt different topologies. These topologies are selected by the algorithm to be presented in Section IV. The goal of this is to force defects having no noticeable effect in the original circuit to have a noticeable effect within the modified topologies.

During the generation of the PXs, two aspects have to be taken into consideration: the sizing of the used transistors and the stress imposed to the circuit when the PXs are activated. After trials on the case study from Section V, it has appeared that the minimal sizing for the PX transistors delivers convincing results. For what concerns the induced stress, the topologies where a current branch exceeds five times the current in the original design are removed from the potential topologies. It is also worth noting that the effects of the capacitive parasitics on the circuit nodes have been neglected. This simplification step has been adopted in order to focus on the core of the method. Instead of this analysis, a pre-selection of the circuit nodes has been made by designers and the sensitive nodes of the circuit have been removed from the circuit nodes to be considered. The method developed in the following is operating on this sub-set of the circuit nodes. In the future, this analysis of the effects of the added parasitics can be automated and included in the method.

B. Local Detection and Transmission System

The Local Detection and Transmission System (LDTS) consists in adding small DfT building blocks in the targeted CUT to enhance the observability of the circuit. As illustrated in Figure 2, these DfT blocks consist of a number of threshold detectors with an embedded threshold detection voltage and an oscillator. These threshold detectors monitor the circuit nodes to verify that the selected node voltages are in their expected range. If a node voltage goes out of its expected range, the threshold detector is triggered and the oscillator is activated. The oscillator leaves a trace in the current consumption which can be detected by the Automated Test Equipment (ATE) outside of the IC, as illustrated in Figure 3. Since the signal is carried in the IC's current consumption, no specific routing for the signal has to be designed and the local routing between the threshold detectors and the oscillator is sufficient.

The threshold detectors are autonomous in the sense that their detection threshold is embedded in their design. The

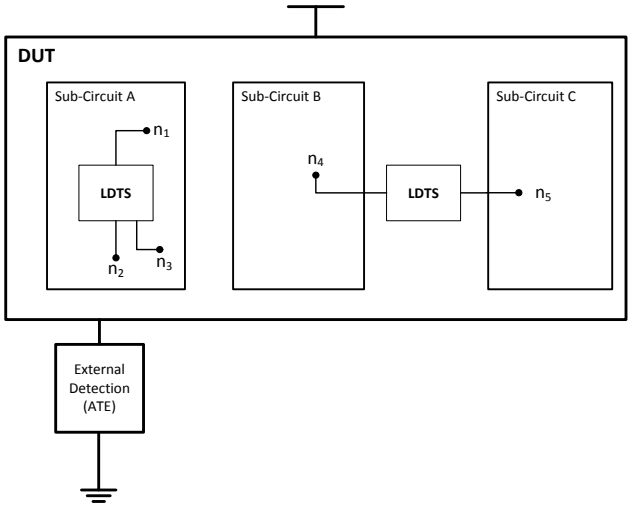

Fig. 3. System-level view of the Local Detection and Transmission [7].

proper sizing of the transistors constituting them allows to define these embedded threshold voltages. This sizing is operated automatically by a simpler optimizer taking process variations into account.

By probing the node voltages and processing the information directly with the threshold detectors, the infrastructures usually needed to bring the node voltages outside the ICs can be avoided. In this way, the required silicon area overhead is significantly reduced. Furthermore, the comparison of the node voltages to their expected range by mean of the threshold detectors is operated in parallel. Therefore, the whole process of scanning the node voltages can be avoided and the test time can be reduced.

IV. Co-optimization Algorithm

Based on the DfT building blocks presented in the previous section, an algorithm is proposed to combine the extra controllability and the extra observability in an optimal way. The target of this optimization is to offer an automatically generated hardware infrastructure testing a given analog IC.

The optimization process relies on the simulations of the faulty circuits generated with the defect-oriented method. These simulations have to include the effects of process variations. However, to ensure the tractability of the method, the process variations can not be simulated for all the faults F_i in the different alternative topologies TM_j. Therefore, the proposed algorithm works in two phases.

During the first phase, simulations are carried out without considering the process variations. The goal is first to choose a selection of the circuit nodes for the topology modification and for the observability enhancement. In the case of the topology modification, nodes offering interesting alternative topologies are searched. In the case of the observability enhancement, nodes where the voltage is different between the good and faulty cases are searched. As stated in Algorithm 1, if for a topology TM_i, a node N_j and a fault F_k, the voltage difference between the faulty case and the good circuit $\parallel V_{ijk}$ - $V_{0jk} \parallel$ is larger than the threshold d, then the 5-uple (i,j,k,V_{0jk},V_{ijk}) is added to the set DB.

During the second phase, based on the set DB, the final selection of topologies and nodes to probe is done by optimization. This optimization looks for a maximal fault coverage and a minimal silicon area. In this work, the required silicon area is simplified in two components counting the number of threshold detectors and the number of modified topologies. This minimization of the number of topologies reduces also the test time. In total, a multi-objective optimization system targeting :

- maximum fault coverage
- minimum number of topologies
- minimum number of threshold detectors

is solved by a genetic algorithm which provides as a result a set of Pareto-optimal solutions.

During this second phase, simulations are carried out in the presence of process variations for the best individuals of the population in the genetic algorithm. This second step allows to assess the effects of the process variations and to select the threshold detectors accordingly. Simulations provide for each node voltage a probability density function instead of a number, and therefore the detection thresholds and their architecture can be refined.

Algorithm 1: Compile information about controllability and observability

Require: Nodes of C_0 $\{N_1, ..., N_m\}$
Require: Available topologies $\{TM_0, ..., TM_p\}$
Require: Faults $\{F_1, ..., F_n\}$
DB= $\emptyset$
for $i = 1, .., p$ **do**
  for $j = 1, .., m$ **do**
    for $k = 1, .., n$ **do**
      if $\parallel V_{ijk}$ - $V_{0jk} \parallel > d$ **then**
        DB=DB $\cup$ (i,j,k,V_{0jk},V_{ijk})
      end if
    end for
  end for
end for

As this multi-objective optimization system targets a maximum fault coverage and a minimal silicon area, the offered solution is not unique but presents a Pareto-optimal set of solutions trading off fault coverage for silicon area. One of these solutions then has to be selected by the test engineer or a tool performing an optimization at system-level.

V. Simulation Results

The proposed method has been applied to the industrial circuit illustrated in Figure 4. This Power-on-Reset (POR) circuit is designed in 0.35μm BCD technology [10]. This circuit is a good candidate for the application of the Topology Modification method. Since it does not have any input besides the power supply voltage, its controllability is very limited. Similarly, the observability offered by the POR is limited. Since the circuit is terminated by a Schmitt Trigger, which presents an inverter at its end, most of the information is filtered out and can never be obtained.

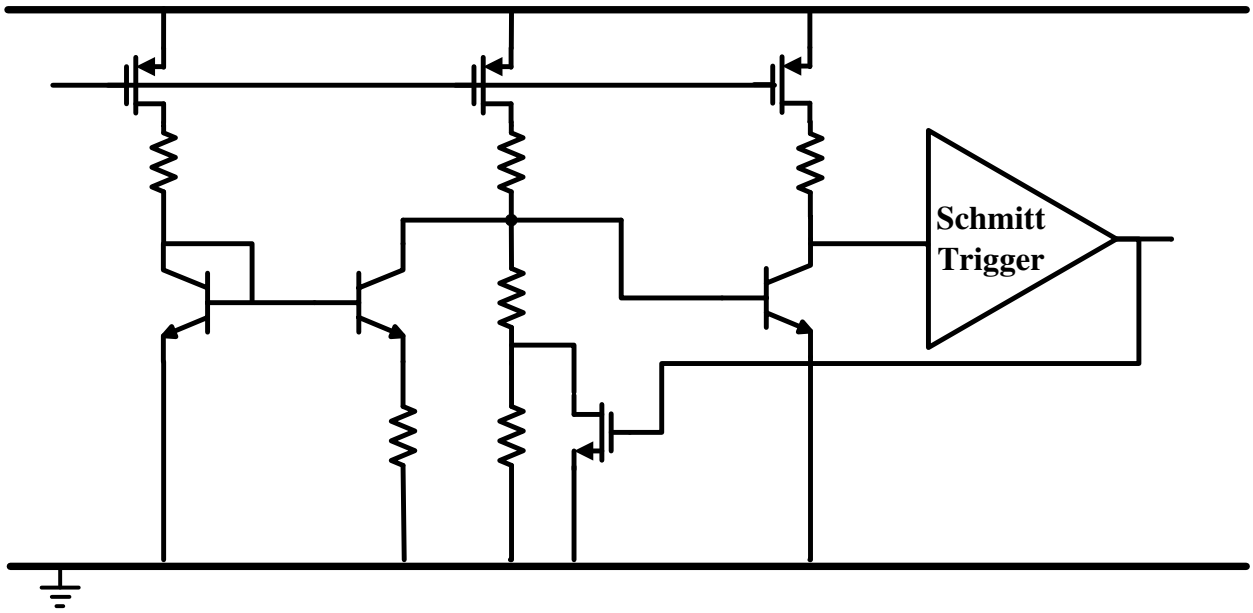

Fig. 4. Block diagram representation of the Power-on-Reset circuit.

Fault Coverage (percent)	Number of threshold detectors	Number of PXs
91.2	4	5
89.7	3	4
88.2	4	3
86.8	2	3
83.8	1	3

TABLE I. FIRST 5 SOLUTIONS IN THE PARETO-OPTIMAL FRONT.

The first step of the defect-oriented method consists in generating the fault list. Based on the fault models introduced in Section II, the 4 bipolar and 12 MOSFET transistors lead to a list of 68 faults. Table I shows different hardware solutions from the Pareto-optimal set produced by the proposed method when applied to the POR circuit. A coverage of 91.2% can be reached with 4 theshold detectors and 5 PXs for an increase of less than 10% in silicon area.

VI. CONCLUSION

In this paper, a method has been proposed where the DfT infrastructure is automatically generated in order to test a given analog circuit. This method uses generic DfT blocks offering extra controllability and extra observability in the circuit under test. An algorithm has been developed to co-optimize this controllability and observability in an optimum way. As a result, a set of Pareto-optimal hardware solutions is proposed, trading off the fault coverage for the required silicon area.

The use of small DfT building blocks instead of an analog scan chain allows here to approach the testing of analog circuits in a general manner but without the drawback of the large area overhead of the analog scan chains. Furthermore, by applying a defect-oriented method, the flow of analog testing has been automated by optimally selecting the required controllability and observability structures in order to test the considered defects.

The proposed method has been applied to an industrial case study and it has been shown that a fault coverage of 91% can be obtained at a silicon area overhead of less than 10%.

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